High Performance Computing

RISC and CISC

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RISC and CISC

RISC Reduced Instruction Set Computers.

CISC Complex Instruction Set Computers.

They describe different hardware architectural designs of a computer, CPU, or computational device balancing the possibility for hardware optimization and power of the instruction set.

Modern RISC and CISC

Modern RISC and CISC designs are much more similar to each other than they were originally.

The two domains have adopted techniques from the respectively other one.

RISC: Reduced Instruction Set Computers

A computer with a small instruction set. The advantage is that the limited complexity allows for better optimization in hardware.

The key feature is that instructions are expected to operate in one cycle, and usually instructions are encoded in fixed length.

The typical example of a RISC design is the RISC-V architecture.

ARM, Sunway, PowerPC, and SPARC are further designs that are usually considered as RISC.

RISC features

Typical features of RISC designs include:

- Fixed format instructions, i.e. operation code is always at the same bit position in a register.
- One instruction per cycle.
- Hardwired instructions as opposed to microcode.
- Efficient pipelining and homogeneous pipelines.
- Simple FPUs as opposed to CPU implementations of square root, sin, etc.
- Largish (homogeneous) register set.

ARM as a RISC design

Some modern ARM designs feature instructions to run Javascript code. Such capabilities would traditionally be expected for CISC designs.

CISC: Complex Instruction Set Computers

A computer with instructions that can decode to several μ-operations or run across several CPU cycles.

Often CISC designs feature variable instruction encoding.

CISC designs are traditionally motivated by the potential of compilers to inject optimized instructions into the code that they generate. In modern context, they are equally tied to application domains.

Translation to μ-operations

Some modern CISC designs translate instructions into μ-operations, which rather adhere to a RISC design.

In this way a CISC design can internally benefit from the optimization potential of RISC designs.

CISC instruction sets

Some of the modern CISC instruction set extensions include:

SEE2 Streaming SIMD Extensions 2.

AVX, AVX2, AVX-512 Advanced vector extension.

AMX Advanced matrix extension.

CISC instruction sets

Operations that can be computed through modern CISC instruction sets include:

- Fused multiplication add: $a \cdot b + c$.
- Vector packed add: $(a_1 + b_1, \ldots, a_8 + b_8)$ for vectors $(a_1, \ldots, a_8)$ and $(b_1, \ldots, b_8)$ stored in one register each.
- Vector packed, horizontal add: $(a_1 + a_2, a_3 + a_4, a_5 + a_6, a_7 + a_8)$ for a vector $(a_1, \ldots, a_8)$ stored in one register.